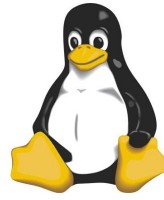


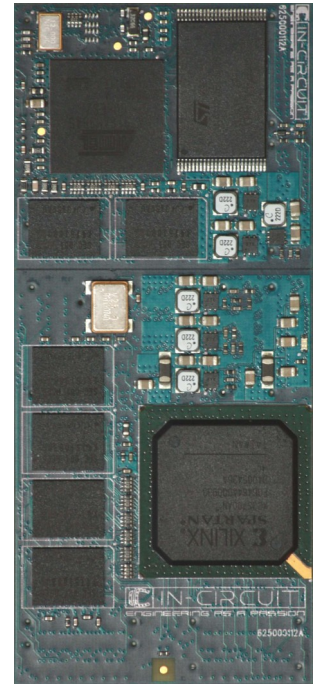
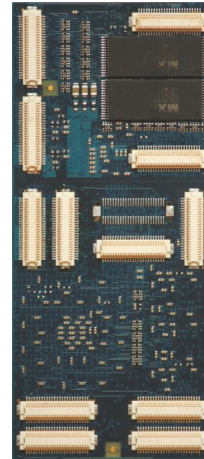
SAM9G45+XC3S700AN Module

- Cost-effective, powerful, reliable
- Guaranteed delivery >5 years (outline contract required)
- Easy design-in at low risk
- Save cost through shorter development cycles
- Starter-kit including ADB3000 and display available

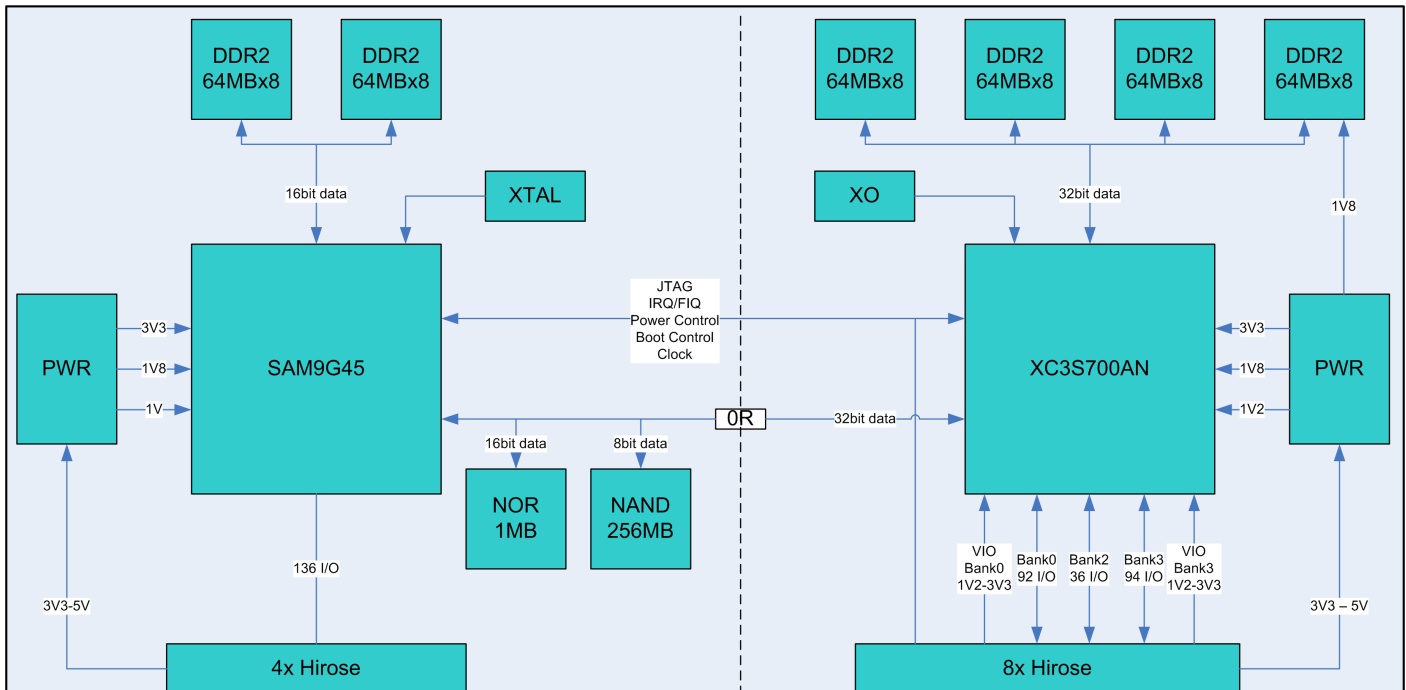


Features

- AT91SAM9G45 processor at 400MHz
 - 32kB data cache, 32kB instruction cache
 - 64kB int. SRAM, 64kB int. ROM
- Xilinx® Spartan XC3S700AN FPGA up to 300MHz
 - 11.776 LUTs/FlipFlops
 - 360kbit internal SRAM
 - 222 I/Os on module connectors
- Memory on the module
 - 128MB DDR2 RAM connected to ARM EBI1
 - 1MB NOR Flash connected to ARM EBI2
 - 256MB NAND connected to ARM EBI2
 - 256MB DDR2 RAM connected to FPGA
- Complete Linux system pre-installed and available as source code
- Direct data connection between ARM and FPGA through 32bit EBI2 SRAM interface
 - Driver for SRAM interface is provided, simple access to FPGA using file I/O
- Completely integrated FPGA reference design included
 - DDR2 RAM controller (royalty-free Xilinx® IP), transfer rates >1GByte/s
 - SRAM interface for control-register and DDR2 access by the ARM
 - GPIO access to all available I/Os
- Configuration and programming the flash of the FPGA by the ARM
 - Driver for the JTAG port is included
 - Configuration of the XC3S700AN from ARM NAND flash within 0.7 seconds
- The complete OEM module runs on a single power supply of between 3.3V and 5V
 - All supplies locally required are created using highly-efficient switching regulators
 - Exception: I/O supplies for FPGA bank 0/3 are directly sourced by the module's connectors in order to enable arbitrary I/O standards
 - At 3.3V I/O supply, the complete board can be supplied by 3.3V
 - Power consumption for the ARM part max 1W
 - FPGA consumption depends on the application, suspend mode available on the Spartan 3AN
 - FPGA power consumption can be reduced to zero by switching off the regulator
- Size (plugged)
 - 90 x 40 x 7 mm, 3.0mm distance board-board
 - Temperature range 0°C to 60°C



Block Diagram



Interface

- Available serial interfaces ARM:
 - 1x 10/100MBit Ethernet (MII)
 - 1x USB 2.0 high speed host (480 MBit)
 - 1x USB 2.0 high speed device (480 MBit)
 - 4x UART + 1x Debug-UART, 1x Synchronous Serial Controller (SSC)
 - 2x SPI, 2x I²C (TWI)
 - 1x AC'97 sound codec interface, 1x high speed Multimedia-Interface (MMI)
 - 4x PWM, 8x ADC, touch screen ADC controller with interrupt signal
 - 1x JTAG
- Available parallel interfaces ARM
 - LCD with max. resolution 2048x2048
 - Image Sensor Interface (ISI)
- All unused signals of the ARM can also be used as GPIO
- The Xilinx® Spartan XC3S700AN FPGA includes 4 I/O banks
 - Bank 1 is completely used up for the DDR2 interface
 - Bank 0, 2 and 3 provide 92, 36 and 94 programmable I/Os on Hirose connectors
 - The voltage of bank 0 and 3 is sourced directly from the Hirose connectors
 - Many I/O standards supported in the range of 1.2V to 3.3V
 - Most of the I/Os can be used either as differential pair or single-ended pin
 - Some of the pins of the FPGA have restrictions regarding direction or diff vs. single
 - The possible I/O configurations are described in more detail on [page 6](#) of this datasheet

Application and Design-In

The ICnova SAM9G45+XC3S700AN OEM module combines

- High processor speed at low power consumption
- High data bandwidth through dedicated DDR2 memory busses on ARM and FPGA
- Huge amounts of DDR2 and flash memory
- Simple design of complex functionality through standard GNU/Linux OS
- Extreme flexibility owing to freely programmable FPGA logic
- Very compact size of only 90mm x 40mm

Achieving high data rates through 100MBit Ethernet or 480MBit USB2.0 is easily possible as well as controlling TFT or LCD displays or accessing periphery via SPI, I2C, UART and many others.

Nearly all signals of the ARM and the FPGA are accessible through the connectors on the bottom side. The memory interfaces are not provided in order to secure their signal integrity. A detailed description of the pins can be found on the following pages.

The ARM section of the SAM9G45+XC3S700AN OEM module is identical to the SAM9G45 OEM module, enabling simple migrations between pure software solutions and software plus FPGA approaches.

Debugging and quality management: During your product development phase, it might happen that hardware components get damaged. Hardware errors in systems using hundreds of I/Os can be hard to find. Included with the SAMG45+XC3S700AN OEM module, you get the complete production test software. This in combination with the ADB3000 enables a complete connectivity test of all I/Os. Shorts or open faults are found and reported in detail.

You need the low latency, high I/O count, data throughput and/or computing power of an FPGA, but want to concentrate on developing your system and software? FPGA design support is available through our competent partner [Loginovo GmbH](#).

Required Tools, Source Codes and Documentation

There is no additional cost for tools, source codes, software or documentation!

- Required Tools

- Linux: All required tools for generating the Linux image are being compiled locally. The corresponding sources are all located on the [ICnova CD](#).
- FPGA: Software for VHDL simulation, synthesis, implementation and bitstream generation is available from Xilinx® ([ISE WebPACK Edition](#)) at no cost.

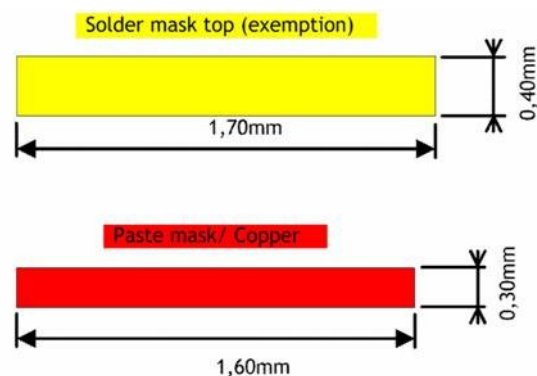
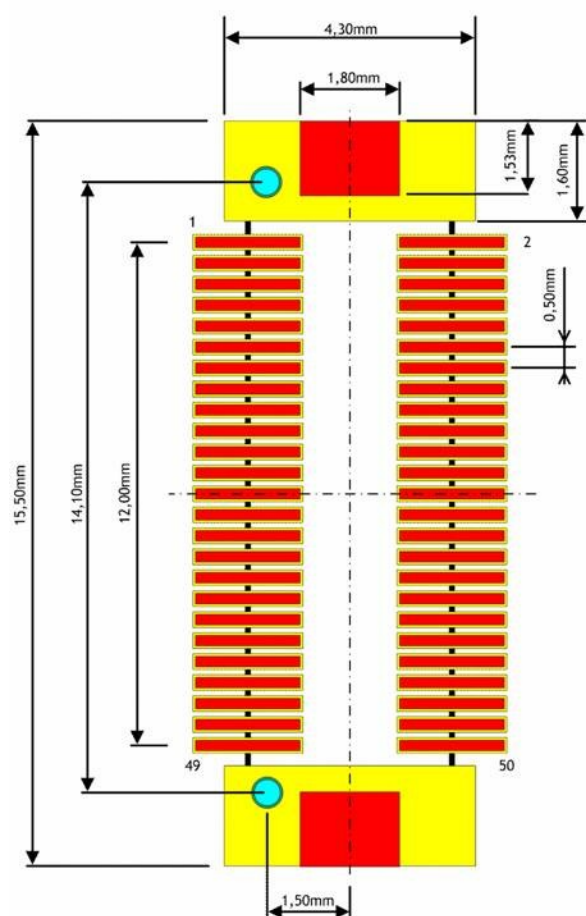
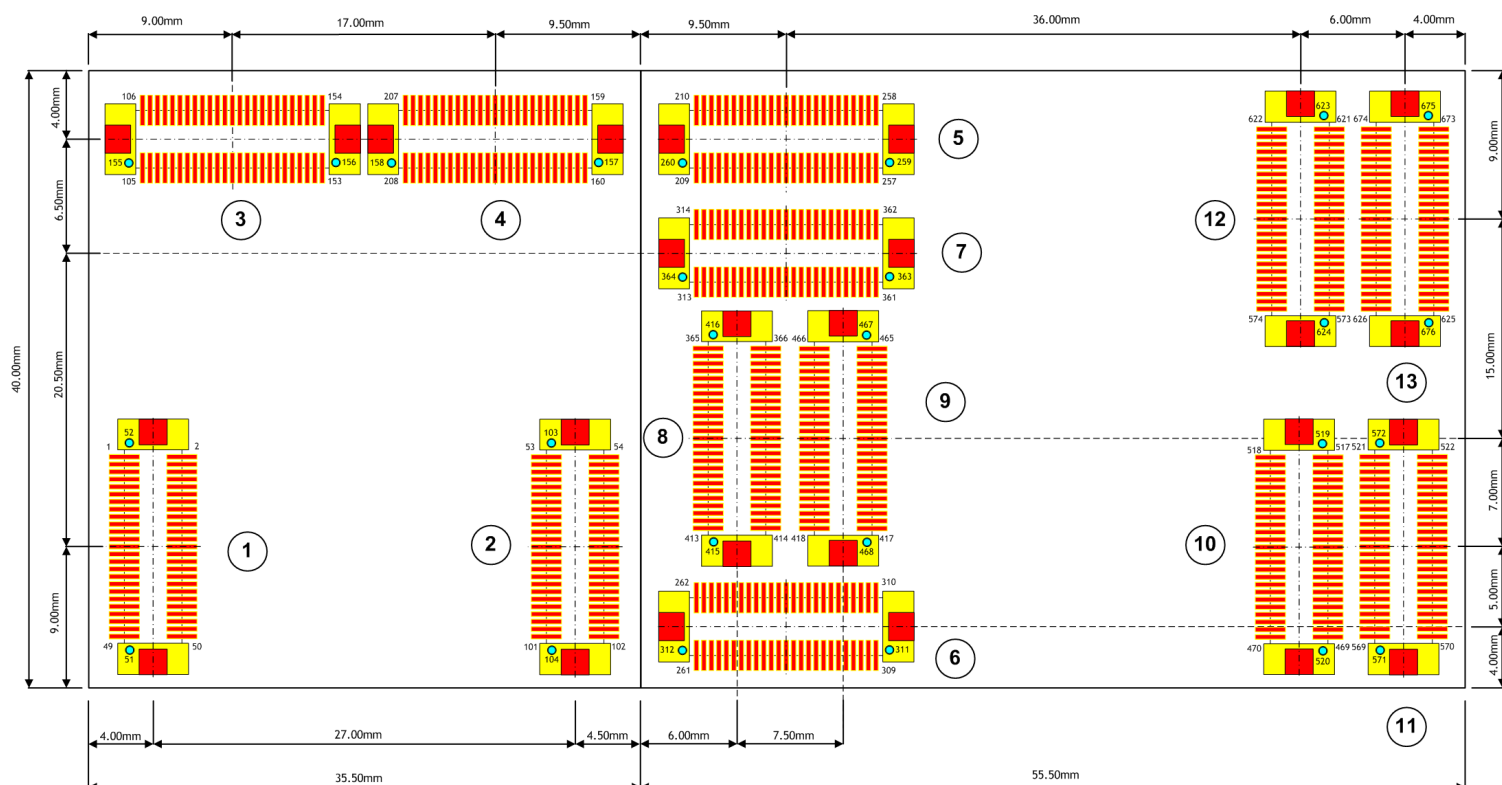
- Software Source Codes

- All sources for creating the Linux image, U-Boot boot loader and the root file system are located on the [ICnova CD](#).
- The driver for accessing the FPGA SRAM interface by the ARM is located on the [ICnova CD](#).
- The driver for programming and writing the flash of the FPGA is made available to ICnova customers in a separate patch in the [ICnova Download Area](#) of Loginovo GmbH. The patch contains source code of a 3rd party and therefore it has to be separated from the open source code of the ICnova CD for legal reasons. Of course the sources and the required customer login are free of charge for customers who have ordered an ICnova SAM9G45+XC3S700AN OEM module or ADB3000 development kit.
- Test software for running the production test on an ADB3000. The sources can also be used as a basis for the customer's own software applications controlling the FPGA. These sources are also located in the [ICnova Download Area](#) of Loginovo GmbH (requires customer login).

- FPGA Design

- The complete VHDL reference design is available in the [ICnova Download Area](#) of Loginovo GmbH (requires customer login). For details regarding the reference design, please take a look at the publicly available reference design spec. The design includes:
 - All required RTL sources for the design
 - Simulation testbench with script-driven stimulators
 - All scripts for simulation and bit stream generation (implementation)
 - Constraint file (UCF) with all pin, logic and timing constraints
- The ICnova FPGA Design Spec documents the functionality and the structure of the reference design. The design includes an SRAM slave interface for the ARM, configuration registers for all GPIOs and the DDR2 SRAM controller. There is a wrapper around the DDR2 controller in order to simplify its utilization for streaming applications. The specification is publicly available in the [ICnova Download Area](#).
- In order to make your design start with the ICnova FPGA as painless as possible, there is an ICnova FPGA HowTo to simplify the first steps. All important steps like 'HowTo simulate' or 'HowTo implement' are being described there. The HowTo is publicly available in the [ICnova Download Area](#).

Footprint using Hirose DF12(3.0)-50DP-0.5V(86)



Drill size non platet hole 0,65mm

Solder mask bottom 0,75mm

solder mask clearance is required, solder resist must not flow into the hole and reduce hole size

FPGA I/O details

The following table lists in detail the number and configuration of available FPGA I/Os per bank. Con 8 includes the 32 data lines of the EB12. This connector is not populated per default in order to protect the signal integrity of this interface.

	Bank 0			Bank 2			Bank 3		
Con	Single input	Diff input	Diff I/O	Single input	Diff input	Diff I/O	Single Input	Diff input	Diff I/O
5									
6	4		4p/8s			2p/4s	2	2p/4s	4p/8s
7	16							8p/16s	
8						16p/32s			
9						16p/32s			
10			16p/32s						
11			16p/32s						
12									16p/32s
13									16p/32s
Sum	20		72			68	2	20	72
Sum: 212 I/Os, 42 inputs, 254 overall									

For the XC3S700AN FPGA, the following restrictions apply:

- „Single input“ pins can be used only as single-ended inputs
- „Diff input“ pin (pairs) may be used as two single inputs or as one differential LVDS input pair
- „Diff I/O“ pin (pairs) can be used as
 - Two single-ended inputs
 - Two single-ended outputs
 - One differential input pair
 - One differential output pair (only bank 0/2, bank 1/3 does not support differential outputs)

Pinout SAM9G45 (con 1 - ARM9)

PIN Hirose connector	Port/Pin ARM9	Periphery on ARM9	Notice
1	GND	GND	
2	PA10	ETX0	
3	PC0	DQM2	
4	PA11	ETX1	
5	PC1	DQM3	
6	PA29	ECRS/MCI1_DA6	
7	GND	GND	
8	PA26	ETH_RESETn/MCI1_DA3/TIOB2	
9	GND	GND	
10	PA30	ECOL/MCI1_DA7	
11	PD31	TIOB1/PWM1	
12	PA25	ETH_PDWN/MCI1_DA2/PWM3	
13	PD30	TIOB0/SCK2	
14	PC6	ETH_MDINTRn/A23	
15	PD28	SPI_NPCS1/TSADTRG	
16	PA27	ETXER/MCI1_DA4	
17	GND	GND	
18	PA6	ETX2/MCI0_DA4	
19	PC0	USB2_PSWN/DQM2	
20	PA7	ETX3/MCI0_DA5	
21	PC1	USB2_OCN/DQM3	
22	PA14	ETXEN	
23	PC0	USB1_PSWN/DQM2	
24	PA17	ETXCK	
25	PC1	USB1_OCN/DQM3	
26	PA12	ERX0	
27	GND	GND	
28	PA13	ERX1	
29	USB-Host3 +		for use, place network resistor R90
30	PA8	ERX2/MCI0_DA6	
31	USB-Host3 -		for use, place network resistor R90
32	PA9	ERX3/MCI0_DA7	
33	GND		
34	PA16	ERXER	
35	USB-Host2 +		for use, place network resistor R89
36	PA28	ERXCK/MCI1_DA5	
37	USB-Host2 -		for use, place network resistor R89
38	PA15	ERXDV	
39	GND		
40	PA19	EMDIO	
41	USB-Host1 +		default USB-Host D+ Pin
42	PA18	EMDC/ETH_MDC	
43	USB-Host1 -		default USB-Host D- Pin
44	GND		
45	GND		
46	GND		
47	PE31	PCK1/PWM2	
48	NC		
49	GND		
50	NC		
51	NC	non plated hole	
52	NC	non plated hole	

Pinout SAM9G45 (con 2 - ARM9)

PIN Hirose connector	Port / Pin ARM9	Periphery on ARM9	Notice
53	PD8	AC97FS/TIOB5	
54	GND		
55	PD7	AS97TX/TIOA5	
56	HHSDMB/DHSDM		Device- or Host- can be selected by Register
57	PD9	AC97CK/TCLK5	
58	HHSDPB/DHSDP		Device+ or Host+ can be selected by Register
59	PD6	AC97RX	
60	GND		
61	PB14	SPI1_MISO	
62	GND		
63	PB31	ISI_MCK/PCK1	
64	GND		
65	GND		
66	GND		
67	GND		
68	TDI		
69	PB11	ISI_DAT11/TWI1_SCL	
70	NTRST		
71	PB10	ISI_D10/TWI1_SDA	
72	NC		
73	PB9	ISI_D9/UART3_RXD	
74	RESETn		
75	PB8	ISI_D8/UART3_TXD	
76	TMS		
77	PB28	ISI_PCLK	
78	TDO		
79	PB29	ISI_VSYNC	
80	TCK		
81	PB30	ISI_HSYNC	
82	GND		
83	PB27	ISI_DAT7	
84	GND		
85	PB26	ISI_DAT6	
86	GND		
87	PB25	ISI_DAT5	
88	PD3	RD0	
89	PB24	ISI_DAT4	
90	PD2	TD0	
91	PB23	ISI_DAT3	
92	PD1	TF0	
93	PB22	ISI_DAT2	
94	GND		
95	PB21	ISI_DAT1	
96	PD0	TK0/PWM3	
97	PB20	ISI_DAT0	
98	PD4	RK0	
99	GND		
100	PD5	RF0	
101	GND		
102	GND		
103	NC	non plated hole	
104	NC	non plated hole	

Pinout SAM9G45 (con 3 - ARM9)

PIN Hirose connector	Port / Pin ARM9	Periphery on ARM9	Notice
105	PE30	LCDD23	
106	GND	GND	
107	PE29	LCDD22	
108	PE23	LCDD16/LCDD22	
109	PE28	LCDD21	
110	PE22	LCDD15/LCDD21	
111	PE27	LCDD20	
112	PE21	LCDD14/LCDD20	
113	GND		
114	PE20	LCDD13/LCDD19	
115	PE26	LCDD19	
116	PE19	LCDD12/LCDD18	
117	PE25	LCDD18	
118	PE18	LCDD11/LCDD15	
119	PE24	LCDD17/LCDD23	
120	PE17	LCDD10/LCDD14	
121	GND		
122	PE16	LCDD9/LCDD13	
123	GND		
124	PE15	LCDD8/LCDD12	
125	PD27	GPAD7/SPI0_NPCS3/PCK1	
126	PE14	LCDD7/LCDD11	
127	PD26	PCK0/PWM2/GPAD6	
128	PE13	LCDD6/LCDD10	
129	GND		
130	PE12	LCDD5/LCDD7	
131	PD23	TCLK0/TSAD3	
132	PE11	LCDD4/LCDD6	
133	PD22	TIOA2/TSAD2	
134	PE10	LCDD3/LCDD5	
135	PD21	TIOA1/TSAD1	
136	PE9	LCDD2/LCDD4	
137	GND		
138	PE8	LCDDAT1/LCDD3	
139	PD20	TIOA0/TSAD0	
140	PE7	LCDD0/LCDD2	
141	PD19	SPI1_NPCS3/FIQ	
142	PE0	LCDPWR/PCK0	
143	PD18	SPI1_NPCS2/IRQ	
144	PE1	LCDDMOD	
145	GND		
146	PE6	LCDDEN/LCDDVAL	
147	PA24	MCI1_DA1/CTS3	
148	PE3	LCDVSYNC	
149	PA23	MCI1_DA0/RTS3	
150	PE5	LCDDOTCK	
151	PA22	MCI1_CDA/SCK3	
152	PE4	LCDHSYNC	
153	GND		
154	PE2	LCDCC	
155	NC	NC	non plated hole
156	NC	NC	non plated hole

Pinout SAM9G45 (con 4 - ARM9)

PIN Hirose connector	Port/Pin ARM9	Periphery on ARM9	Notice
157	NC	NC	non plated hole
158	NC	NC	non plated hole
159	ARM9_EN		enables voltage regulators, connect to VCC for normal operation
160	VCC_ARM9		+3.3V-5V
161	VCC_ARM9		+3.3V-5V
162	VCC_ARM9		+3.3V-5V
163	VCC_ARM9		+3.3V-5V
164	VCC_ARM9		+3.3V-5V
165	VCC_ARM9		+3.3V-5V
166	VCC_ARM9		+3.3V-5V
167	GND		
168	GND		
169	GND		
170	GND		
171	GND		
172	GND		
173	GND		
174	GND		
175	WKUP	WAKEN	use a 10K pullup
176	GND		
177	NRST	RESET_OUT	use a button to ground for reset
178	PB16	SPI1_SPCK/SCK0	
179	PD29	TCLK1/SCK1	
180	PB18	RXD0/SPI0_NPCS1	
181	PB5	RXD1	
182	PB19	TXD0/SPI0_NPCS2	
183	GND		
184	PB15	CTS0/SPI1_MOSI	
185	PB4	TXD1	
186	PB17	RTS0/SPI1_NPCS0	
187	PD16	RTS1	
188	GND		
189	PD17	CTS1	
190	PB6	TXD2	
191	GND		
192	PB7	RXD2	
193	PB12	DRXD	
194	PA20	TWD0	
195	PB13	DTXD	
196	PA21	TWCK0	
197	PB0	SPI0_MISO	
198	PA0	MCIO_CK/TCLK3	
199	PB1	SPI0_MOSI	
200	PA1	MCIO_CDA/TIOA3	
201	PB2	SPI0_SCK	
202	PA2	MCIO_DA0/TIOB3	
203	PB3	SPI0_NPCS0	
204	PA3	MCIO_DA1/TCLK4	
205	PD24	SPI0_NPCS1/PWM0/GPAD4	
206	PA4	MCIO_DA2/TIOA4	
207	PD25	SPI0_NPCS2/PWM1/GPAD5	
208	PA5	MCIO_DA3/TIOB4	

Pinout XC3S700AN (con 5 - supply+JTAG)

PIN Hirose connector	BALL NAME	Signal Name	Notice
209	VCC_FPGA		+3.3V-5V
210	VCC_FPGA		+3.3V-5V
211	VCC_FPGA		+3.3V-5V
212	VCC_FPGA		+3.3V-5V
213	VCC_FPGA		+3.3V-5V
214	FPGA_En		enables voltage regulators, connect to VCC for normal operation
215	VCC_FPGA		+3.3V-5V
216	GND		
217	VCC_FPGA		+3.3V-5V
218	F5	TDI	
219	VCC_FPGA		+3.3V-5V
220	A21	TCK	
221	VCC_FPGA		+3.3V-5V
222	GND		
223	VCC_FPGA		+3.3V-5V
224	E19	TDO	
225	VCC_FPGA		+3.3V-5V
226	D4	TMS	
227	VCCO_3		+3.3V
228	GND		
229	VCCO_3		+3.3V
230	V13	FPGA_INITB/ IO_L26P	
231	VCCO_3		+3.3V
232	Y19		
233	VCCO_3		+3.3V
234	GND		
235	VCCO_3		+3.3V
236	GND		
237	VCCO_3		+3.3V
238	GND		
239	VCCO_3		+3.3V
240	GND		
241	VCCO_3		+3.3V
242	GND		
243	VCCO_0		+3.3V
244	GND		
245	VCCO_0		+3.3V
246	GND		
247	VCCO_0		+3.3V
248	GND		
249	VCCO_0		+3.3V
250	GND		
251	VCCO_0		+3.3V
252	GND		
253	VCCO_0		+3.3V
254	GND		
255	VCCO_0		+3.3V
256	GND		
257	VCCO_0		+3.3V
258	GND		
259	NC	non plated hole	
260	NC	non plated hole	

Pinout XC3S700AN (con 6 - bank 0/2/3 I/Os)

PIN Hirose connector	BALL NAME	Signal Name	Notice
261	GND		
262	GND		
263	AA1	IO_L45P_3	
264	U18	SUSPEND	high input for suspend mode activation (only if bit is set)
265	AA2	IO_L45N_3	
266	C4	PROG_B	
267	GND		
268	GND		
269	Y1	IO_L44P_3	
270	AB15	IO_L24P_2/Awake	awake is a open-drain output (the default), if suspend mode is active
271	Y2	IO_L44N_3	
272	AA15	IO_L24N_2/DOUT	
273	GND		
274	GND		
275	V4	IO_L43P_3	
276	U11	IO_L17P_2/GCLK12	
277	W3	IO_L43N_3	
278	V11	IO_L17N_2/GCLK13	
279	GND		
280	GND		
281	W1	IO_L42P_3	
282	J7	IP_L11P_3	
283	W2	IO_L42N_3	
284	K8	IP_L11N_3	
285	GND		
286	GND		
287	B2	IO_L36P_0	
288	H8	IP_L04P_3	
289	A2	IO_L36N_0/PDUC_B	
290	H7	IP_L04N_3/VREF_3	
291	GND		
292	GND		
293	F7	IO_L35P_0	
294	J8	IP02_3/VREF_3	
295	E6	IO_L35N_0	
296	R6	IP01_3/VREF_3	
297	GND		
298	GND		
299	E7	IO_L34P_0	
300	F12	IP04_0	
301	F8	IO_L34N_0	
302	F10	IP03_0	
303	GND		
304	GND		
305	A3	IO_L33P_0	
306	E8	IP02_0	
307	B3	IO_L33N_0	
308	E16	IP01_0	
309	GND		
310	GND		
311	NC	non plated hole	
312	NC	non plated hole	

Pinout XC3S700AN (con 7 - bank0+3 inputs)

PIN Hirose connector	BALL NAME	Signal Name	Notice
313	GND		
314	GND		
315	H9	IP20_0/VREF_0	
316	R7	IP_L46P_3	
317	H12	IP19_0/VREF_0	
318	T6	IP_L46N_3/VREF_3	
319	GND		
320	GND		
321	G8	IP18_0/VREF_0	
322	P7	IP_L39P_3	
323	H14	IP17_0	
324	R8	IP_L39N_3	
325	GND		
326	GND		
327	H13	IP16_0	
328	N7	IP_L35P_3	
329	H10	IP15_0	
330	P8	IP_L35N_3	
331	GND		
332	GND		
333	G9	IP14_0	
334	N6	IP_L31P_3	
335	G7	IP13_0	
336	N5	IP_L31N_3	
337	GND		
338	GND		
339	G16	IP12_0	
340	N8	IP_L27P_3	
341	G15	IP11_0	
342	N9	IP_L27N_3	
343	GND		
344	GND		
345	G14	IP10_0	
346	M7	IP_L23P_3	
347	G13	IP09_0	
348	M6	IP_L23N_3	
349	GND		
350	GND		
351	G12	IP08_0	
352	L7	IP_L19P_3	
353	G11	IP07_0	
354	M8	IP_L19N_3	
355	GND		
356	GND		
357	G10	IP06_0	
358	K7	IP_L15P_3	
359	F16	IP05_0	
360	L8	IP_L15N_3/VREF_3	
361	GND		
362	GND		
363	NC	non plated hole	
364	NC	non plated hole	

Pinout XC3S700AN (con 8 - bank2 I/O)*

PIN Hirose connector	BALL NAME	Signal Name	Notice
365	GND		
366	GND		
367	AA17	IO_L28P_2/D2	
368	AB20	IO_L36P_2/D0/DIN/MISO	
369	Y17	IO_L28N_2/D1	
370	AA20	IO_L36N_2/CCLK	
371	GND		
372	GND		
373	AB16	IO_L27P_2	
374	AB21	IO_L35P_2	
375	Y16	IO_L27N_2	
376	AA21	IO_L35N_2	
377	GND		
378	GND		
379	W15	IO_L25P_2	
380	Y18	IO_L34P_2	
381	Y15	IO_L25N_2	
382	W17	IO_L34N_2	
383	GND		
384	GND		
385	W13	IO_L23P_2	
386	W18	IO_L33P_2	
387	Y14	IO_L23N_2	
388	V17	IO_L33N_2	
389	GND		
390	GND		
391	AA14	IO_L22P_2	
392	AB19	IO_L32P_2	
393	AB14	IO_L22N_2/MOSI/CSI_B	
394	AA19	IO_L32N_2	
395	GND		
396	GND		
397	AB13	IO_L21P_2	
398	W16	IO_L31P_2	
399	Y13	IO_L21N_2	
400	V16	IO_L31N_2	
401	GND		
402	GND		
403	V12	IO_L20P_2/GCLK2	
404	V14	IO_L30P_2	
405	U12	IO_L20N_2/GCLK3	
406	V15	IO_L30N_2	
407	GND		
408	GND		
409	W12	IO_L18P_2/GCLK14	
410	AB17	IO_L29P_2	
411	Y12	IO_L18N_2/GCLK15	
412	AB18	IO_L29N_2	
413	GND		
414	GND		
415	NC	non plated hole	
416	NC	non plated hole	

* This connector is only available when the ARM9 on the OEM module is not used

Pinout XC3S700AN (con 9 - bank2 I/O)

PIN Hirose connector	BALL NAME	Signal Name	Notice
417	GND		
418	GND		
419	AA6	IO_L08P_2	
420	Y11	IO_L16P_2/D5	
421	AB6	IO_L08N_2	
422	AB11	IO_L16N_2/D4	
423	GND		
424	GND		
425	W7	IO_L07P_2	
426	AA10	IO_L15P_2	
427	Y6	IO_L07N_2	
428	AB10	IO_L15N_2	
429	GND		
430	GND		
431	AB4	IO_L06P_2	
432	Y9	IO_L14P_2/D7	
433	AB5	IO_L06N_2	
434	AB9	IO_L14N_2/D6	
435	GND		
436	GND		
437	W6	IO_L05P_2	
438	V10	IO_L13P_2	
439	Y5	IO_L05N_2	
440	Y10	IO_L13N_2	
441	GND		
442	GND		
443	AB3	IO_L04P_2	
444	AA8	IO_L12P_2	
445	AA4	IO_L04N_2	
446	AB8	IO_L12N_2	
447	GND		
448	GND		
449	AB2	IO_L03P_2	
450	W8	IO_L11P_2/VS1	
451	AA3	IO_L03N_2	
452	Y8	IO_L11N_2/VS0	
453	GND		
454	GND		
455	W4	IO_L02P_2/M2	
456	Y7	IO_L10P_2	
457	Y4	IO_L02N_2/CSO_B	
458	AB7	IO_L10N_2	
459	GND		
460	GND		
461	V6	IO_L01P_2/M1	
462	V9	IO_L09P_2/RDWR_B	
463	W5	IO_L01N_2/M0	
464	W9	IO_L09N_2/VS2	
465	GND		
466	GND		
467	NC	non plated hole	
468	NC	non plated hole	

Pinout XC3S700AN (con 10 - bank0 I/O)

PIN Hirose connector	BALL NAME	Signal Name	Notice
469	GND		
470	GND		
471	D16	IO_L08P_0	
472	B13	IO_L16P_0	
473	C16	IO_L08N_0	
474	A13	IO_L16N_0	
475	GND		
476	GND		
477	D17	IO_L07P_0	
478	D13	IO_L15P_0	
479	C17	IO_L07N_0	
480	C13	IO_L15N_0	
481	GND		
482	GND		
483	B19	IO_L06P_0/VREF_0	
484	F13	IO_L14P_0	
485	A19	IO_L06N_0	
486	E13	IO_L14N_0	
487	GND		
488	GND		
489	C18	IO_L05P_0	
490	B15	IO_L13P_0	
491	A18	IO_L05N_0	
492	A14	IO_L13N_0	
493	GND		
494	GND		
495	E15	IO_L04P_0	
496	A16	IO_L12P_0	
497	F15	IO_L04N_0	
498	A15	IO_L12N_0/VREF_0	
499	GND		
500	GND		
501	B20	IO_L03P_0	
502	D15	IO_L11P_0	
503	A20	IO_L03N_0	
504	C15	IO_L11N_0	
505	GND		
506	GND		
507	D19	IO_L02P_0/VREF_0	
508	B17	IO_L10P_0	
509	C19	IO_L02N_0	
510	A17	IO_L10N_0	
511	GND		
512	GND		
513	E17	IO_L01P_0	
514	C14	IO_L09P_0	
515	D18	IO_L01N_0	
516	E14	IO_L09N_0	
517	GND		
518	GND		
519	NC	non plated hole	
520	NC	non plated hole	

Pinout XC3S700AN (con 11 - bank0 I/O)

PIN Hirose connector	BALL NAME	Signal Name	Notice
521	GND		
522	GND		
523	B9	IO_L24P_0	
524	C5	IO_L32P_0	
525	C9	IO_L24N_0/VREF_0	
526	D5	IO_L32N_0	
527	GND		
528	GND		
529	D10	IO_L23P_0	
530	A4	IO_L31P_0	
531	E10	IO_L23N_0	
532	B4	IO_L31N_0	
533	GND		
534	GND		
535	A9	IO_L22P_0	
536	E9	IO_L30P_0	
537	A8	IO_L22N_0	
538	D8	IO_L30N_0	
539	GND		
540	GND		
541	A10	IO_L21P_0	
542	C6	IO_L29P_0	
543	C10	IO_L21N_0	
544	D6	IO_L29N_0	
545	GND		
546	GND		
547	D11	IO_L20P_0/GCLK10	
548	B6	IO_L28P_0	
549	E11	IO_L20N_0/GCLK11	
550	A5	IO_L28N_0	
551	GND		
552	GND		
553	B11	IO_L19P_0/GCLK8	
554	D7	IO_L27P_0	
555	C11	IO_L19N_0/GCLK9	
556	C7	IO_L27N_0	
557	GND		
558	GND		
559	A12	IO_L18P_0/GCLK6	
560	A7	IO_L26P_0	
561	A11	IO_L18N_0/GCLK7	
562	A6	IO_L26N_0	
563	GND		
564	GND		
565	C12	IO_L17P_0/GCLK4	
566	B8	IO_L25P_0	
567	E12	IO_L17N_0/GCLK5	
568	C8	IO_L25N_0	
569	GND		
570	GND		
571	NC	non plated hole	
572	NC	non plated hole	

Pinout XC3S700AN (con 12 - bank3 I/O)

PIN Hirose connector	BALL NAME	Signal Name	Notice
573	GND		
574	GND		
575	M5	IO_L30P_3	
576	U3	IO_L41P_3	
577	N4	IO_L30N_3	
578	U4	IO_L41N_3	
579	GND		
580	GND		
581	P3	IO_L29P_3	
582	T5	IO_L40P_3	
583	P5	IO_L29N_3	
584	U5	IO_L40N_3	
585	GND		
586	GND		
587	P1	IO_L28P_3	
588	V1	IO_L38P_3	
589	P2	IO_L28N_3	
590	V3	IO_L38N_3	
591	GND		
592	GND		
593	N1	IO_L26P_3/VREF_3	
594	U1	IO_L37P_3	
595	N3	IO_L26N_3	
596	U2	IO_L37N_3	
597	GND		
598	GND		
599	M3	IO_L25P_3/TRDY2/LHCLK6	
600	T1	IO_L36P_3/VREF_3	
601	M4	IO_L25N_3/LHCLK7	
602	T3	IO_L36N_3	
603	GND		
604	GND		
605	M1	IO_L24P_3/LHCLK4	
606	R5	IO_L34P_3	
607	M2	IO_L24N_3/LHCLK5	
608	T4	IO_L34N_3	
609	GND		
610	GND		
611	K1	IO_L22P_3/LHCLK2	
612	R3	IO_L33P_3	
613	L1	IO_L22N_3/IRDY2/LHCLK3	
614	R4	IO_L33N_3	
615	GND		
616	GND		
617	L5	IO_L21P_3/LHCLK0	
618	R1	IO_L32P_3	
619	L3	IO_L21N_3/LHCLK1	
620	R2	IO_L32N_3	
621	GND		
622	GND		
623	NC	non plated hole	
624	NC	non plated hole	

Pinout XC3S700AN (con 13 - bank3 I/O)

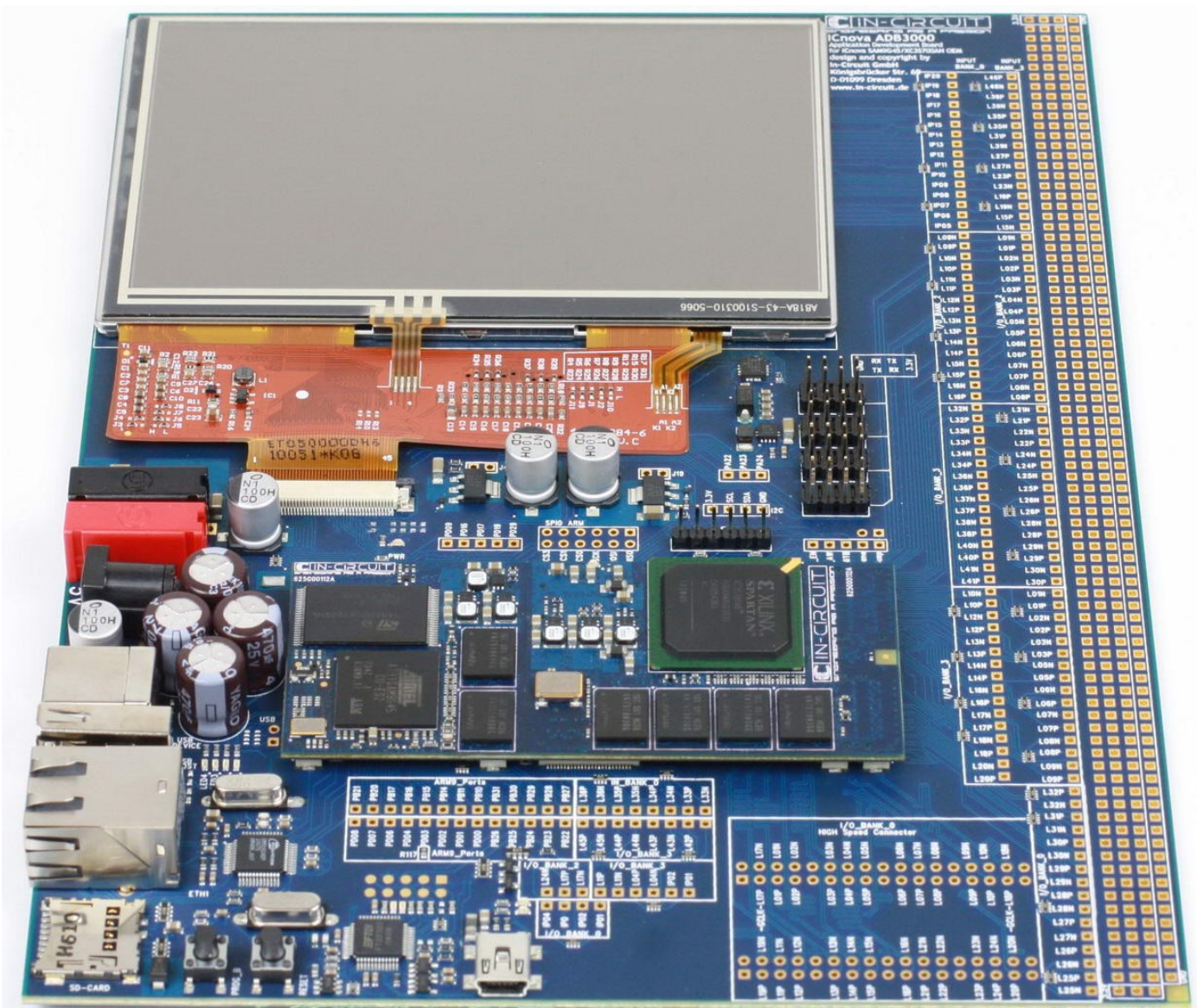
PIN Hirose connector	BALL NAME	Signal Name	Notice
625	GND		
626	GND		
627	H5	IO_L09P_3	
628	K3	IO_L20P_3	
629	H6	IO_L09N_3	
630	K2	IO_L20N_3	
631	GND		
632	GND		
633	F3	IO_L08P_3	
634	K5	IO_L18P_3	
635	G4	IO_L08N_3	
636	K4	IO_L18N_3	
637	GND		
638	GND		
639	F4	IO_L07P_3	
640	J3	IO_L17P_3	
641	E3	IO_L07N_3	
642	J1	IO_L17N_3/VREF_3	
643	GND		
644	GND		
645	D1	IO_L06P_3	
646	H2	IO_L16P_3	
647	E1	IO_L06N_3	
648	H1	IO_L16N_3	
649	GND		
650	GND		
651	G6	IO_L05P_3	
652	H4	IO_L14P_3	
653	G5	IO_L05N_3	
654	H3	IO_L14N_3	
655	GND		
656	GND		
657	D3	IO_L03P_3	
658	G3	IO_L13P_3	
659	E4	IO_L03N_3	
660	G1	IO_L13N_3	
661	GND		
662	GND		
663	B1	IO_L02P_3	
664	F2	IO_L12P_3	
665	C2	IO_L02N_3	
666	F1	IO_L12N_3	
667	GND		
668	GND		
669	C1	IO_L01P_3	
670	K6	IO_L10P_3	
671	D2	IO_L01N_3	
672	J5	IO_L10N_3	
673	GND		
674	GND		
675	NC	non plated hole	
676	NC	non plated hole	

Evaluation and Development

Complementary to the ICnova SAM9G45+XC3S700AN OEM, we offer the evaluation board ADB3000 and a corresponding starter kit with OEM board and 5" display. Among others, the ADB3000 offers the following features:

- All FPGA I/Os available on pin headers
- Two high-speed connectors with 12 differential pairs each plus ground
- Integrated OpenOCD debugger und debug-UART for ARM via mini-USB connector
- Power supply can be done using a wall power supply, a lab supply using banana jacks or USB
- Ethernet, μ SD, USB Host, USB Slave and many more...

More details can be found in the ADB3000 datasheet.



Ordering information			
Description	Article number	Packaging	Min order quantity
ICnova SAM9G45+XC3S700AN	901.180	ESD-bag, air cushion	1

Besides corresponding evaluation boards, we also offer:

- Hardware design of base boards optimized for your application
- Prototype and mass production using our internal production lines
- Adaptation / assembly options of our standard products
- Linux driver development and adaptation

FPGA design services including integration with corresponding (test-) software are available through our competent partner [Loginovo GmbH](#).



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Change history

Version	Date	Changes	Editor
A	08/25/2010	First version	Gassmann
B	09/15/2010	Added page for required software, source codes and documentation	Gassmann
D	09/16/2011	Inserted corrected footprint, distance between connector 8 and 9 was wrong. Stopped maintaining German version.	Gassmann
E	01/27/2012	Corrected name of pin 270 (awake), was named 24N, but is 24P. Translated remaining german footnote on page 14 to English. Flip-ped Con9 pins, were mirrored before.	Gassmann