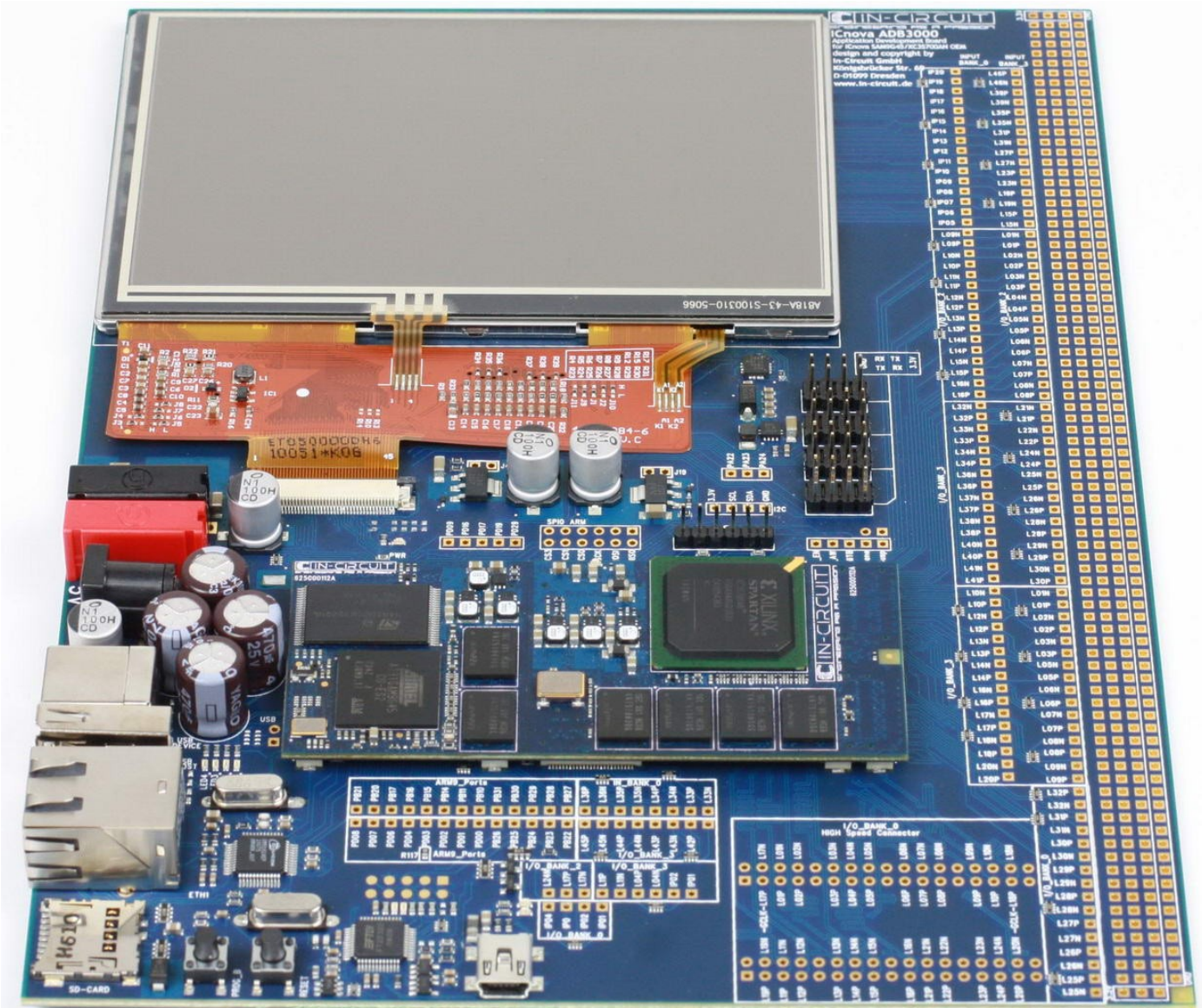


## ICnova-ADB3000

The development platform for your embedded Linux + FPGA projects:

- Optimized for the SAM9G45+XC3S700AN OEM module, compatible to all ICnova OEM modules
- All spare FPGA and ARM I/Os are available on pin headers
- Two high-speed connectors with 12 differential pairs each plus ground
- Integrated OpenOCD debugger und debug-UART for ARM via mini-USB connector
- No additional cables or adapters are necessary in order to program the ARM and the FPGA, all that is needed is an Ethernet cable and a USB port
- Power supply can be done using a wall power supply, a lab supply using banana jacks or USB
- Size: 200 x 220.13mm
- Temperature range 0°C to 60°C



This picture shows the ADB3000 equipped with a SAM9G45+XC3S700AN OEM and a 5" display

## Interfaces ARM

- 10/100MBit Ethernet
- USB 2.0 high speed host (480 MBit)
- USB 2.0 high speed device (480 MBit)
- UART0/1/2 and DBGUART on pin headers
- UART3 via mini USB plug
  - virtual COM-port on the host
  - ADB3000 Linux image uses this UART for the boot terminal
  - LEDs for RX/TX activity
- SPI with 3x chip selects
- I<sup>2</sup>C (TWI)
- µSD/MMC card slot
- OpenOCD JTAG adapter via mini USB plug
  - Tunnels through the same USB port as UART3
  - No additional programming adapters are required
- JTAG ICE MKII, not populated per default owing to the on-board OpenOCD adapter
- LCD touchscreen interface
- 4 LEDs, for example for indicating kernel heartbeat and flash disk access
- 34 GPIOs on pin headers, in addition many of the other interfaces may be alternatively used as GPIOs
- Reset button

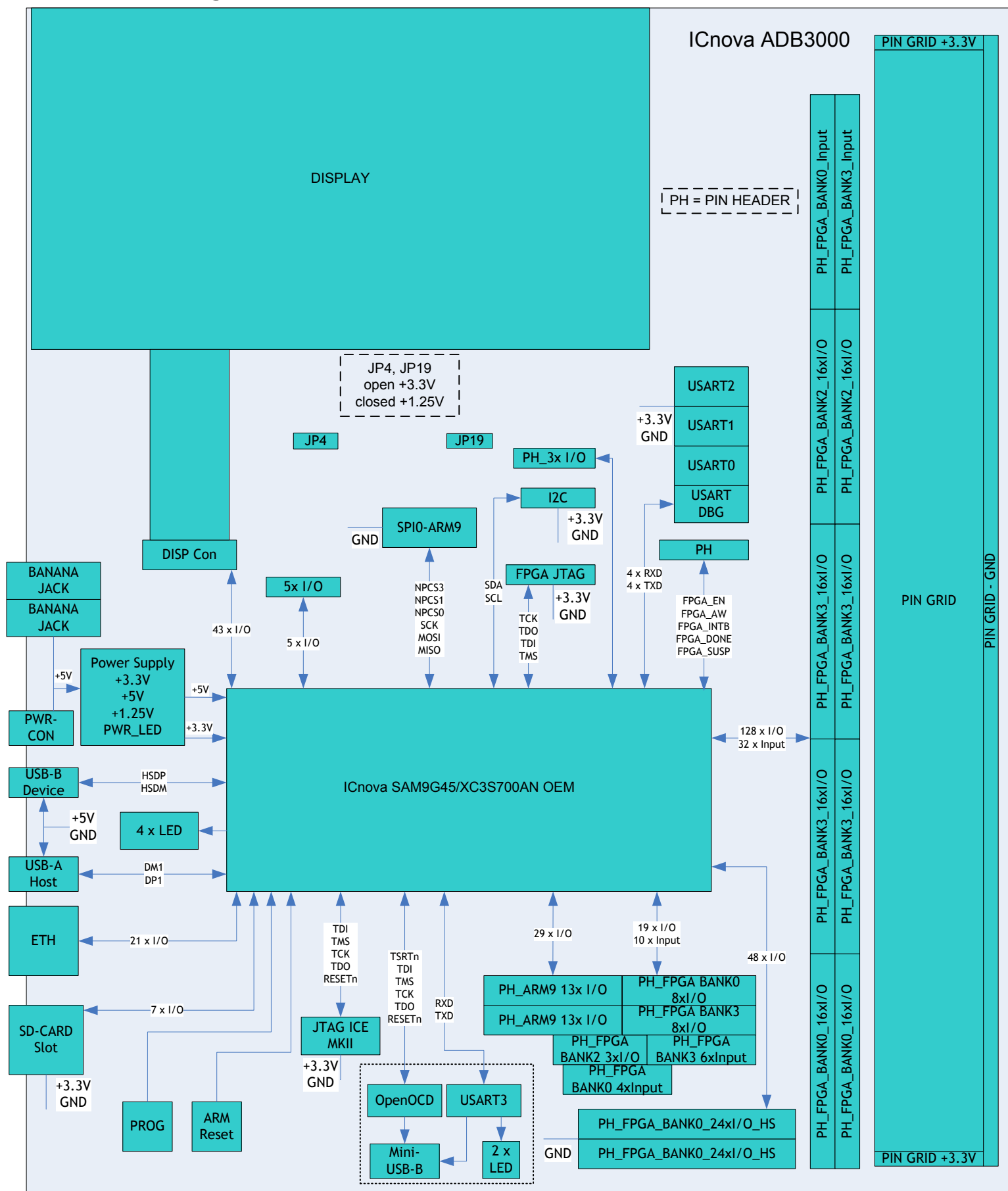
## Interfaces FPGA

- 222 I/Os on pin headers, organized on the board as follows:
  - Bank0: (4x12)xI/Os high-speed, (16+8)xI/O, (16+4)xinput
  - Bank1: No I/Os available, all required for DDR2 RAM interface
  - Bank2: (32+3+1)xI/O, FPGA\_Awake pin can be used as I/O
  - Bank3: (4x16+6+8)xI/O, 16xinput
- JTAG on pin header
  - Not needed for configuration or flashing, however required for Xilinx® Chipscope™
  - Configuration and writing the FPGA's flash can be done by the ARM
- Low-Power / programming interface on pin header
  - Enable/Disable pin for FPGA voltage regulator
  - FPGA Suspend /Awake
  - INIT/DONE pins
- PROG-button for re-configuration
- 2 LEDs connected to I/Os bank2 L17P/N

## Power Supply

- Only one power supply of 5V is required. This one is connected directly to
  - the OEM board socket
  - the USB host / device plugs
- On-board are being generated from the 5V:
  - 3.3V for board components like display, Ethernet PHY, LEDs etc
  - I/O supplies for FPGA I/O bank0 and bank3
- The I/O supply voltages for I/O bank0 and bank3 are adjustable using jumper J4 and J19
  - Jumper open: 3.3V
  - Jumper closed: 1.25V
  - Using a resistor, the voltages can be adjusted between 1.25V and 3.3V
  - Examples: 1.5V (51Ω), 1.8V (130Ω) or 2.5V (220Ω).
- The I/O supply voltages of banks 1 and 2 are fixed to
  - 1.8V for DDR2 interface (bank1)
  - 3.3V for ARM SRAM interface (bank2)
- The supply can be done through the following connectors:
  - Coaxial power connector (GND on outer contact)
  - Banana plugs
  - USB-B device plug (keep in mind the maximum USB current!)
  - Mini USB-B plug for OpenOCD and UART3 (keep in mind the maximum USB current!)
  - Using a wall power or lab supply is recommended
- Power consumption / requirements to supply
  - The power consumption of the board with inactive display and FPGA is around 1W
  - Beyond that, the supply is heavily dependent on the FPGA design in use
  - With a fully loaded FPGA DDR2 interface, the consumption can exceed 4W
  - It is discouraged to supply the ADB3000 via USB when the FPGA is in use
  - USB provides only  $4.75V \cdot 0.5A = 2.375W$  according to the USB standard
  - **Supply via USB may destroy your host!**

## Block Diagram



## Required Tools, Source Codes and Documentation

There is no additional cost for tools, source codes, software or documentation!

- Required Tools

- Linux: All required tools for generating the Linux image are being compiled locally. The corresponding sources are all located on the [ICnova CD](#).
- FPGA: Software for VHDL simulation, synthesis, implementation and bitstream generation is available from Xilinx® ([ISE WebPACK Edition](#)) at no cost.

- Software Source Codes

- All sources for creating the Linux image, U-Boot boot loader and the root file system are located on the [ICnova CD](#).
- The driver for accessing the FPGA SRAM interface by the ARM is located on the [ICnova CD](#).
- The driver for programming and writing the flash of the FPGA is made available to ICnova customers in a separate patch in the [ICnova Download Area](#) of Loginovo GmbH. The patch contains source code of a 3rd party and therefore it has to be separated from the open source code of the ICnova CD for legal reasons. Of course the sources and the required customer login are free of charge for customers who have ordered an ICnova SAM9G45+XC3S700AN OEM module or ADB3000 development kit.
- Test software for running the production test on an ADB3000. The sources can also be used as a basis for the customer's own software applications controlling the FPGA. These sources are also located in the [ICnova Download Area](#) of Loginovo GmbH (requires customer login).

- FPGA Design

- The complete VHDL reference design is available in the [ICnova Download Area](#) of Loginovo GmbH (requires customer login). For details regarding the reference design, please take a look at the publicly available reference design spec. The design includes:
  - All required RTL sources for the design
  - Simulation testbench with script-driven stimulators
  - All scripts for simulation and bit stream generation (implementation)
  - Constraint file (UCF) with all pin, logic and timing constraints
- The ICnova FPGA Design Spec documents the functionality and the structure of the reference design. The design includes an SRAM slave interface for the ARM, configuration registers for all GPIOs and the DDR2 SRAM controller. There is a wrapper around the DDR2 controller in order to simplify its utilization for streaming applications. The specification is publicly available in the [ICnova Download Area](#).
- In order to make your design start with the ICnova FPGA as painless as possible, there is an ICnova FPGA HowTo to simplify the first steps. All important steps like 'HowTo simulate' or 'HowTo implement' are being described there. The HowTo is publicly available in the [ICnova Download Area](#).

| Ordering information |                |                      |                    |
|----------------------|----------------|----------------------|--------------------|
| Description          | Article number | Packaging            | Min order quantity |
| ICnova ADB3000       | 902.101        | ESD-bag, air cushion | 1                  |

We also offer the following services:

- Hardware design of base boards optimized for your application
- Prototype and mass production using our internal production lines
- Adaptation / assembly options of our standard products
- Linux driver development and adaptation

FPGA design services including integration with corresponding (test-) software are available through our competent partner [Loginovo GmbH](#).



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## Change history

| Version | Date       | Changes                                             | Editor   |
|---------|------------|-----------------------------------------------------|----------|
| A       | 09/06/2010 | First version                                       | Gassmann |
| B       | 09/15/2010 | Added page for source code, tools and documentation | Gassmann |
|         |            |                                                     |          |
|         |            |                                                     |          |
|         |            |                                                     |          |
|         |            |                                                     |          |